APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,829	09/05/2003	Yiqun Lin	125.082US01	7154

7590	02/21/2006	EXAMINER

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ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/655,829	LIN ET AL.
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>03</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>01/06/2006</u>.

2a) ☒ This action is **FINAL.**   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-32</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-32</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____.

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Responsive to communication application 10/655,829 filed on 09/05/2003 and

Applicant Argument filed on 01/06/2006, claims 1-32 are pending.

Claims 1-2, 11, 13, 22-23, and 30 have been amended.

2.   Applicant's arguments, see page 2, filed 01/06/2006, the specification is

amended. Applicant's Abstract is approved.

3.   Applicant's arguments, with respect to Claim Objections have been fully

considered and are persuasive.

4.   Applicant's arguments filed 01/06/2006 have been fully considered but they are

not persuasive. Therefore, the claim rejections are maintained.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6.   **Claims 1-32 are rejected under 35 U.S.C. 102(e) as being anticipated by**

Smith et al. (Smith) (US 2003/0229875).

7.   **With respect to claims 1, 11, and 22,** Smith discloses a computer system and

method (abstract) of simulating a layout of an integrated circuit, comprising:

(claims 1, 11, and 22) automatically identifying (determining) empty areas in a layout that can be filled (pg. 3, ¶ 26, col.1, ll. 7-9; col. 2, ll.1-4; and ll. 18-19); and

(claims 1, 11, and 22) generating fill patterns to fill the empty areas (pg. 3, ¶ 26, col. 1, ll. 12-25 and col. 2, ll.1-4; and ll. 18-19) using (claim 11, based at least in part on) a recursive partition (repeatedly dividing) algorithm (fig. 9, ¶ 26 and ¶ 124 – dividing a layout into grids; and fig. 24, step [34-2-7-8-1] though step [34-2-7-8-9], ¶ 203, a loop which is the algorithm determining if there is area still available for fill, then the remaining fill area is divided into a new region and placed it. The dividing step [34-2-7-8-8] is repeated until there is not available fill area --).

8.   **With respect to claims 2 and 23**, Smith discloses the method of claims 1 and 22, respectively further comprising: automatically filling the empty areas with the fill patterns (pg. 3, ¶ 26, col. 2, ll.1-4; and ll. 18-19).

9.   **With respect to claims 3, 18, and 24**, Smith discloses the method of claims 1, 11, and 22, respectively further comprising:

selecting the fill patterns (pg. 3, ¶ 26, col.1, ll. 22-25 and col. 2, ll.27-30 – generating pattern model, which is selected dependence empty areas in layout extraction, and pg. 7, ¶ 114, ll. 4-9);

placing the pattern in empty areas to fill the empty areas (pg. 3, ¶ 26, col. 2, ll.1-4; and ll. 18-19).

10.   **With respect to claims 4 and 14**, Smith discloses the method of claims 1 and 11, respectively further comprising: filling select empty areas with the fill patterns (pg. 3, ¶ 26, col. 2, ll.1-4; and ll. 18-19; pg. 7, ¶ 114, ll. 4-9).

11.   **With respect to claims 5 and 25**, Smith discloses the method of claims 1 and

22, respectively further comprising: defining a unique layout cell for each fill pattern that

is placed in a designated library (pg. 7, ¶ 114, ll. 13-28).

12.   **With respect to claims 6 and 26**, Smith discloses the method of claims 1 and

22, respectively further comprising: using a configuration file to define the fill pattern (fig.

20B and it description; pg. 12, ¶ 187; and pg. 11, ¶ 176 – using the Canonical

interconnect structure to generate (define) the fill pattern).

13.   **With respect to claims 7, 15-17, 19-21, and 27**, Smith discloses all the

limitations as set forth claims:

       wherein automatically identifying empty areas in a layout that can be filled (pg. 3,

¶ 26, col.1, ll. 7-9; col. 2, ll.1-4; and ll. 18-19), further comprises:

       running the empty area identification design tool that is based on design rule

checking (DRC) requirements (pg. 7, ¶ 114, ll. 12-29 – generating design rule and

constraint then convert them to dummy fill (empty fill) guidelines. The complete system

ran until a dummy fill is determined that meets the desired process specification--).

       when the design does not pass the DRC test (pg. 7, ¶ 114, ll. 1 – if the design

does not meet the specified tolerance (design rule) --), modifying the design layout, the

empty areas and fill pattern (pg. 7, ¶ 114, ll. 2-9 – adjusting (modifying) the layout and

the size of dummy fill and fill pattern --).

14.   **With respect to claims 8 and 28**, Smith discloses the method of claims 1 and

22, respectively further comprising: using a hierarchical database that is adapted to

provide easy modification or move-ability of fill patterns (fig. 19 and 24, and see their description, pg. 12, ¶ 188, ll. 6-15).

15.   **With respect to claims 9 and 31**, Smith discloses the method of claims 1 and 22, respectively further comprising: filling select empty areas with the fill patterns, wherein the select empty areas represent different layers of mask and metal in the integrated circuit (fig. 2A and 2B and see their description; and pg.1, ¶ 6-8)

16.   **With respect to claims 10 and 32**, Smith discloses the method of claims 9 and 31, respectively further comprising: wherein at least one of the different layers is filled with different shape fill patterns than the shapes in fill patterns of the other different layers (pg. 12, ¶ 180).

17.   **With respect to claims 12 and 29**, Smith discloses the method of claims 11 and 22, respectively further comprising: wherein the empty areas are represent as polygon (pg. 12, ¶ 179 – mathematically square is one type of polygon--)

18.   **With respect to claims 13 and 30**, Smith discloses the method of claims 12 and 29, wherein the recursive partition (repeated dividing) algorithm on select empty areas to partition the select empty areas into multiple rectangles to be filled with the fill patterns (fig. 9, ¶ 26 and ¶ 124 – dividing a layout into grids; and fig. 24, step [34-2-7-8-1] though step [34-2-7-8-9], ¶ 203, a loop which is the algorithm determining if there is area still available for fill, then the remaining fill area is divided into a new region and placed it. The dividing step [34-2-7-8-8] is repeated until there is not available fill area --
).

Response to Arguments

19.   Applicant's arguments filed 01/06/2006 have been fully considered but they are

not persuasive:

On page 8, Applicant state "Smith reference does not teach a recursive partition

algorithm".

Examiner respectfully does not agree for the following reason:

At figure 9 and ¶ 26, Smith discloses the step divided a layout of dummy filed into

grid, and figure 24 step [34-2-7-8-1] though step [34-2-7-8-9] and ¶ 203, Smith also

discloses repeatedly dividing remaining dummy fill areas into a new region (step [43-2-

7-8-8]) until there is not available fill area (step [34-2-7-8-9]). This disclosure reads on

the claim language of using a recursive partition algorithm. Therefore, the claim

rejections are maintained.

Conclusion

20.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

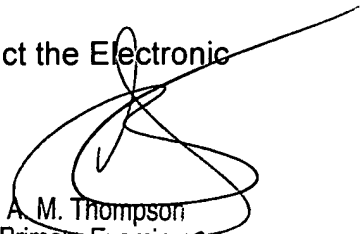extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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